Agilent Technologies
B4655A FPGA Dynamic Probe

Data sheet

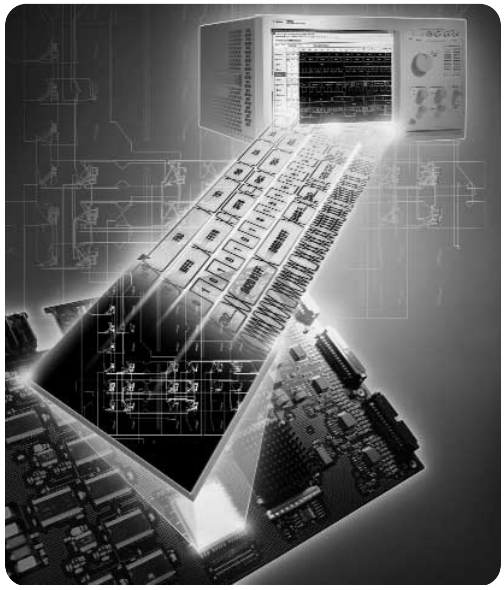
The Challenge

You rely on the insight a logic analyzer provides to understand the behavior of your FPGA in the context of the surrounding system. A typical approach is to take advantage of the programmability of the FPGA to route internal nodes to a small number of physical pins that a logic analyzer can measure. While this is a very useful approach, it has significant limitations.

- Since pins on the FPGA are typically an expensive resource, there are a relatively small number available for debug. This limits internal visibility (i.e. one pin is required for each internal signal to be probed).
- When different internal signals need to be accessed you must change your design to route these signals to pins. This can be time consuming and can affect the timing of the FPGA design.
- Finally, the process required to map the signal names from the FPGA design to the logic analyzer setup is manual and tedious. When new signals are routed out, the need to manually update these signal names on the logic analyzer takes additional time and is a potential source of confusing errors.

A Better Way

Collaborative development between Agilent and Xilinx have produced a faster and more effective way to use your logic analyzer to debug FPGAs and the surrounding system. The Agilent FPGA dynamic probe, used in conjunction with an Agilent logic analyzer, provides the most effective solution for simple through complex debugging.



Overall Winner
EE ProductCenter Reader's Choice Awards

Best of Show

Agilent Technologies

Debug your FPGAs faster and more effectively with a logic analyzer

The Agilent FPGA dynamic probe, used in conjunction with an Agilent logic analyzer, provides the most effective solution for debugging problems [simple through complex]. The FPGA dynamic probe lets you:

- *View internal activity* — With a logic analyzer, you are normally limited to measuring signals at the periphery of the FPGA. With the FPGA dynamic probe, you can now access signals internal to the FPGA. You can measure up to 64 internal signals for each external pin dedicated to debug, unlocking visibility into your design than you never had before.

- *Make multiple measurements in seconds* — Moving probe points internal to an FPGA used to be time consuming. Now, in less than a second you can easily measure a different set of internal signals — without design changes. FPGA timing stays constant when you select new sets of internal signals for probing.

- *Leverage the work you did in your design environment* — The FPGA dynamic probe is the industry's first tool that maps internal signal names from your FPGA design tool to your logic analyzer. Eliminate unintentional mistakes and save hours of time with this automatic setup of signal and bus names on your logic analyzer.

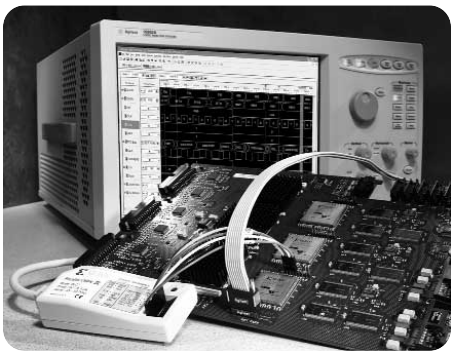


Figure 1. The FPGA dynamic probe application endows your logic analyzer with unique productivity enhancements to find problems more quickly.

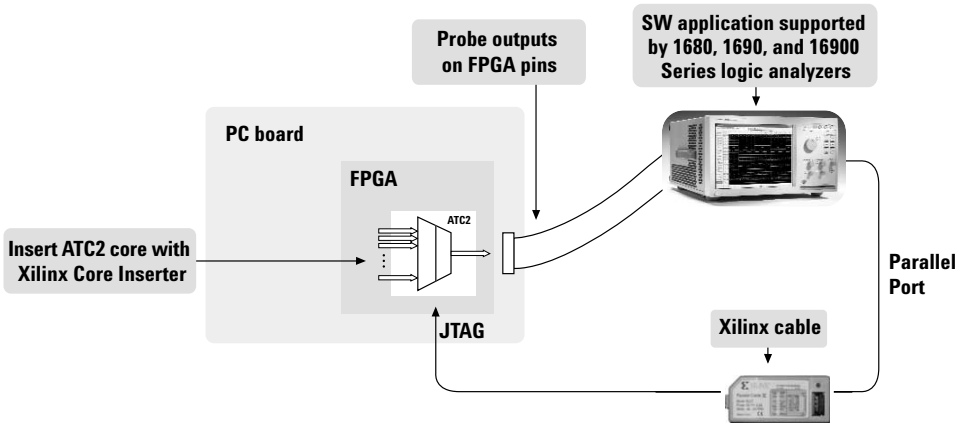


Figure 2. Create a timesaving FPGA measurement system. Insert an ATC2 (Agilent Trace Core) core into your FPGA design. With the application running on your logic analyzer via JTAG you control which group of internal signals to measure.

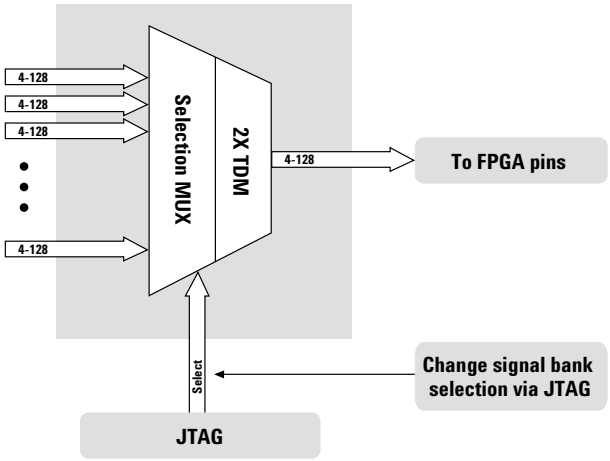
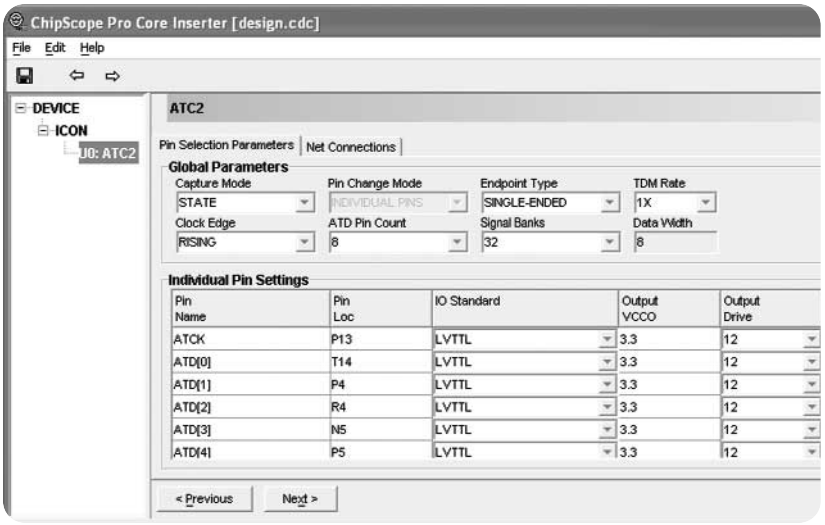


Figure 3. Access up to 64 internal signals for each debug pin. Select cores with 1, 2, 4, 8, 16, or 32 signal banks. Signal banks all have identical width (4 to 128 signals wide) determined by the number of pins you devote for debug. Each pin provides sequential access to 1 signal on every input bank. Using an optional 2X time division compression in state mode, each pin can simultaneously access 2 signals per bank.

A quick tour of the application

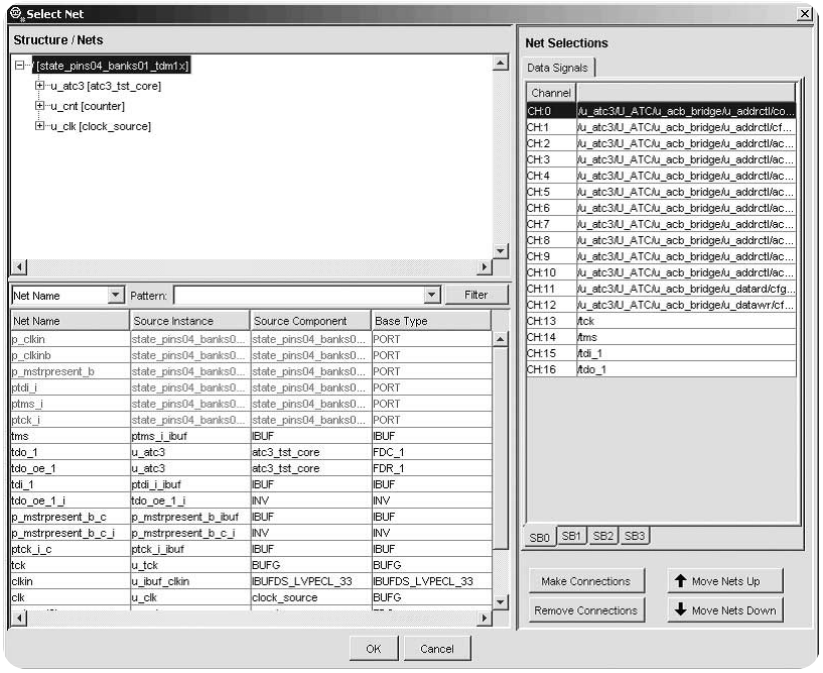
Design step 1: Create the ATC2 core

Use Xilinx Core Inserter to select your ATC2 parameters and to create a debug core that best matches your development needs. Parameters include number of pins, number of signal banks, and the type of measurement (state or timing).



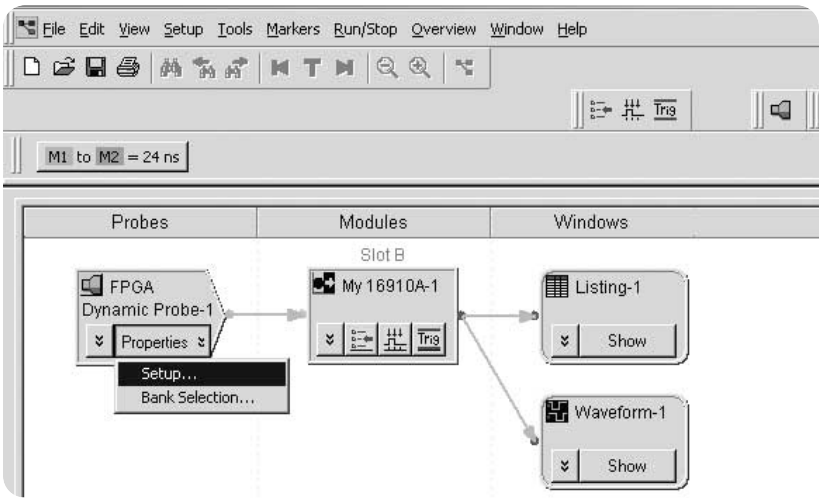
Design step 2: Select groups of signals to probe

Specify banks of internal signals that are potential candidates for logic analysis measurements (using Xilinx Core Inserter).



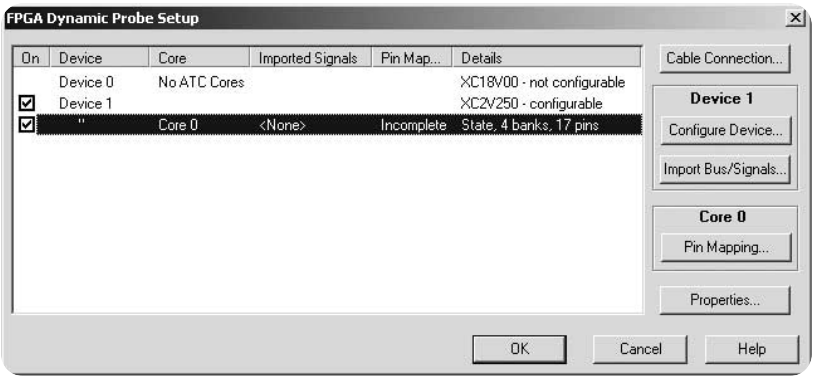
Activate FPGA Dynamic Probe

The FPGA dynamic probe icon allows you to control the ATC2 Core and setup the logic analyzer.



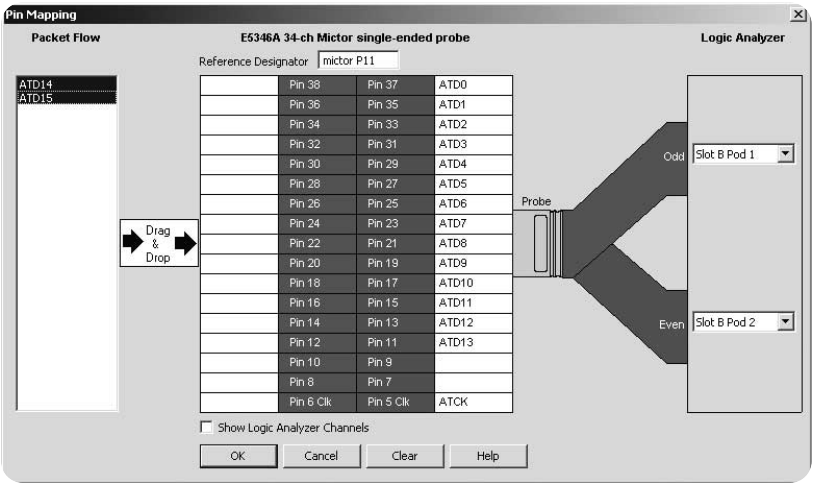
Measurement setup step 1: Establish a connection between the analyzer and the ATC2 core

The FPGA dynamic probe application establishes a connection between the logic analyzer and a Xilinx cable. It also determines what devices are on the JTAG scan chain and lets you pick which one you wish to communicate. Core and device names are user definable.



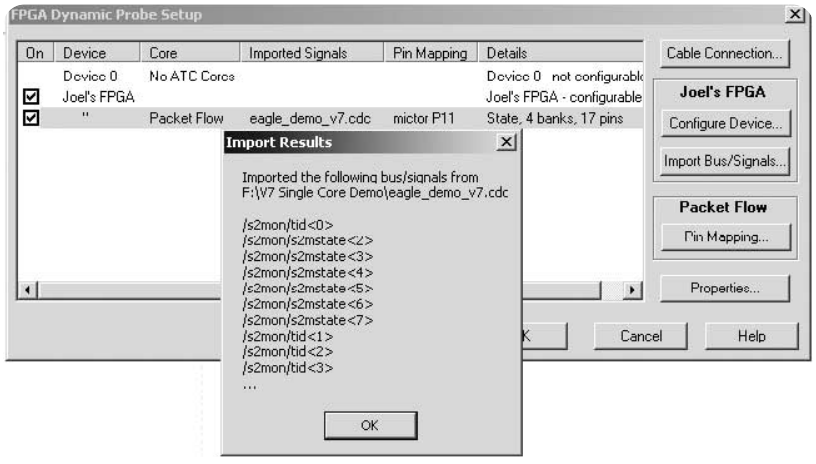
Measurement setup step 2: Map FPGA pins

Quickly specify how the FPGA pins (the signal outputs of ATC2) are connected to your logic analyzer. Select your probe type and rapidly provide the information needed for the logic analyzer to automatically track names of signals routed through the ATC2 core.

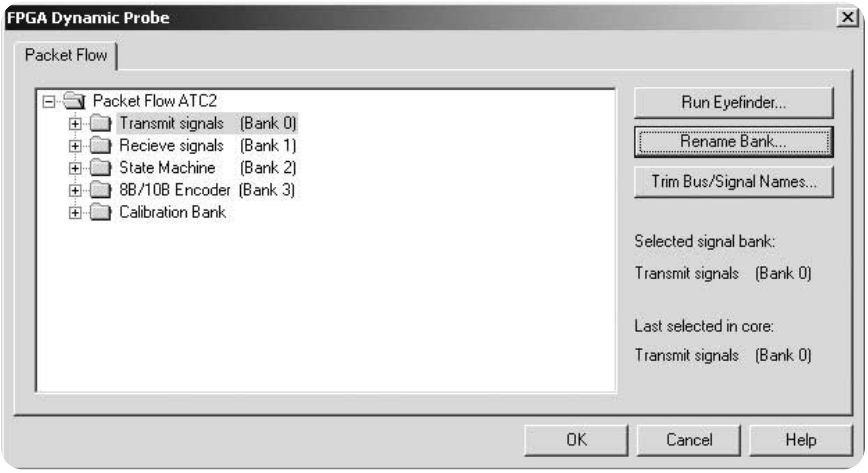


Measurement setup step 3: Import signal names

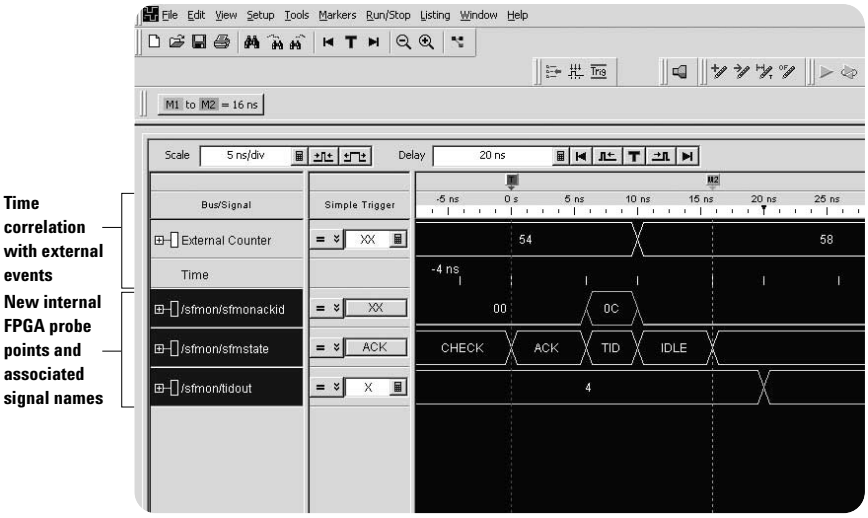
Tired of manually entering bus and signal names on your logic analyzer? In seconds, the FPGA dynamic probe application reads a .cdc file produced by Xilinx Core Inserter. The names of signals you measure will now automatically show on your logic analysis interface.



Setup Complete: Make measurements
Quickly change which signal bank is routed to the logic analyzer. A single mouse click tells the ATC2 core to switch to the newly specified signal bank without any impact to the timing of your design. To make measurements throughout your FPGA, change signal banks as often as needed. User-definable signal bank names make it straight forward to select a part of your design to measure.



Correlate internal FPGA activity with external measurements
With each new selection of an signal bank, the application updates new signal names from your design to the logic analyzer. View internal FPGA activity and time correlate internal FPGA measurements with external events in the surrounding system.



Using the FPGA Dynamic probe, each pin provides access to up to 64 internal signals. The number of debug pins can range from 4 to 128 depending on your needs. When using synchronous cores, one additional pin is used for the clock.

Number of debug pins	Maximum internal signals
4	256
8	512
16	1024
32	2048
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.	.
.	.
128	8192

Agilent B4655A specifications and characteristics

Supported logic analyzers	
Standalone logic analyzers (version 2.5 or higher software)	1680A/AD, 1681A/AD, 1682A/AD, 1683A/AD 1690A/AD, 1691A/AD, 1692A/AD, 1693A/AD
Modular logic analysis systems (version 2.5 or higher software)	16900A, 16902A, 16903A with one or more of the following modules: • 16740A, 16741A, 16742A • 16750A/B, 16751A/B, 16752A/B, 16753A, 16754A, 16755A, 16756A • 16910A, 16911A, 16950A A single FPGA dynamic probe license will enable all modules within a 16900 Series system
Triggering capabilities	Determined by logic analyzer
Supported Xilinx FPGA families	Virtex-4, Virtex-II Pro series, Virtex-II series, Spartan-3 series
Supported Xilinx cables (required)	Parallel 3 and 4
Supported probing mechanisms	Soft touch (34-channel and 17-channel), Mictor, Samtec, Flying lead

FPGA dynamic probe software application	
Maximum number of devices supported on a JTAG scan chain	256
Maximum number of ATC2 cores supported per FPGA device	15

Agilent trace core characteristics	
Number of output signals	User definable: Clock line plus 4 to 128 signals in increments of 1 signal
Signal banks	User definable: 1, 2, 4, 8, 16, or 32
Modes	State (synchronous) or timing (asynchronous) mode
Compression	Optional 2X compression in state mode via time division multiplexing. Logic analyzer decompresses the data stream to allow for full triggering and measurement capability.
FPGA Resource consumption	Approximately 1 slice required per input signal to ATC2 Core Consumes no BUFGs, DCM or Block RAM resources. See resource calculator at www.agilent.com/find/fpga_FAQ

Compatible design tools	
Xilinx ChipScope Pro (required)	Xilinx Core Inserter Version 6.2i or higher Xilinx Core Generator Version 6.2i or higher
Xilinx ISE	Version 6.2i or higher
Synthesis	Core Inserter produces ATC2 cores post-synthesis (pre-place and route) making the cores synthesis independent. ATC2 cores produced by Core Generator are compatible with: • Exemplar Leonardo Spectrum • Synopsys Design Compiler • Synopsys Design Compiler II • Synopsys FPGA Express • Synplicity Synplify • Xilinx XST

Additional information available via the Internet (www.agilent.com/find/FPGA) and www.agilent.com/find/fpga_FAQ.

Ordering information

The Agilent B4655A FPGA dynamic probe includes:

Option 010

- Entitlement certificate for 1-year node-locked license. A single license supports all modules within a 16900 Series system.
- Entitlement certificate for 1-year software update and support services
- CD with application software

Option 011

- Entitlement certificate for perpetual node-locked license. A single license supports all modules within a 16900 Series system.
- Entitlement certificate for 3-year software update and support services
- CD with application software

Related Literature

Publication Title	Publication Type	Publication Number
Agilent Technologies 16900 Series Logic Analysis Systems	Color Brochure	5989-0420EN
Agilent Technologies Timing and State Modules for the 16900 Series	Data Sheet	5989-0422EN
Probing Solutions for Agilent Technologies Logic Analyzers	Catalog	5966-4632E
Agilent 1680 and 1690 Series Logic Analyzers	Data Sheet	5988-2675EN
FPGA Dynamic Probe	Data Sheet	5989-1593EN

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